<table>
<thead>
<tr>
<th>Module Code</th>
<th>CSU22022</th>
</tr>
</thead>
<tbody>
<tr>
<td>Module Name</td>
<td>COMPUTER ARCHITECTURE I</td>
</tr>
<tr>
<td>ECTS Weighting</td>
<td>5 ECTS</td>
</tr>
<tr>
<td>Semester taught</td>
<td>Semester 2</td>
</tr>
<tr>
<td>Module Coordinator/s</td>
<td>Lecturing Prof. Michael Manzke, chief examiner Prof. Michael Manzke</td>
</tr>
</tbody>
</table>

### Module Learning Outcomes

On successful completion of this module, students will be able to:

- **LO1.** design substantial logic circuits using register transfer descriptions;
- **LO2.** test and verify their design using an industry standard hardware description language (VHDL);
- **LO3.** understand the organisation and execution behaviour of general-purpose processor systems;

### Module Content

Specific topics addressed in this module include:

- Digital Logic
- Register transfer language
- ALU and shifter design
- Multiplexer and tristate busses.
- Datapath design
- Instruction fetch-decode-execute cycle

### Teaching and Learning Methods

The lectures and tutorials teach the detailed design and organisation of microprocessor.

**Course Work:** One project using VHDL and a simulator to simulate and test the student’s design. The project has three milestones:

1. Registerfile design and simulation,
2. A processor unit (ALU + shifter + fast registers) design and simulation,
3. An instruction processor design and simulation.

**Contents:** Digital Logic, Register transfer definition, micro-operations, bus transfers, ALU design, shifter design, hardwired control design, microprogrammed processor control, design of an instruction processor.

The aims of the course are to learn register-transfer specification and design and learn the fundamentals of an instruction processor.

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1. TEP Glossary
## Assessment Details

<table>
<thead>
<tr>
<th>Assessment Component</th>
<th>Brief Description</th>
<th>Learning Outcomes Addressed</th>
<th>% of total</th>
<th>Week set</th>
<th>Week due</th>
</tr>
</thead>
<tbody>
<tr>
<td>Examination</td>
<td>written examination</td>
<td>LO1, LO2, LO3</td>
<td>80%</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>Coursework</td>
<td>One Assignment</td>
<td>LO1, LO2, LO3</td>
<td>20%</td>
<td>3/5/9</td>
<td>4/8/12</td>
</tr>
</tbody>
</table>

### Reassessment Details

- e.g. Examination (2 hours, 100%)

### Contact Hours and Indicative Student Workload

- **Contact Hours (scheduled hours per student over full module), broken down by:**
  - lecture: 26 hours
  - tutorial: 8 hours
  - other: 0 hours

- **Independent study (outside scheduled contact hours), broken down by:**
  - preparation for classes and review of material (including preparation for examination, if applicable): 40 hours
  - completion of assessments (including examination, if applicable): 50 hours

- **Total Hours:** 125 hours

### Recommended Reading

- Logic and Computer Design Fundamentals

### Module Pre-requisites

- **Prerequisite modules:** None

### Module Co-requisites

- None

### Module Website


### Last Update

- 01/08/2019 by Michael Manzke

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2 [TEP Guidelines on Workload and Assessment](#)