Write a Verilog behavioural description

    module Compare (A, B, Y);

of a four-bit unsigned comparator with a six-bit output Y[5:0].

Bit 5 of Y is for “equals,” bit 4 for “not equal to,” bit 3 for “greater than,” bit 2 for “less than,” bit 1 for “greater than or equal,” and bit 0 for “less than or equal to.”