Using continuous assignments, write a Verilog module Circuit_2 (Out_1, Out_2, Out_3, A, B, C, D); for the circuit specified by the following Boolean functions:

\[
Out_1 = (A + B')C'(C + D)
\]
\[
Out_2 = (C'D + BCD + CD')(A' + B)
\]
\[
Out_3 = (AB + C)D + B'C
\]