Design an 8 bit serial 2’s complementer with a shift register and a flip-flop. The binary number is shifted out from one side and its 2’s complement shifted into the other side of the shift register.

module Serial_Twos_Comp (output y, input [7: 0] data, input load, shift_control, Clock, reset_b);

Test data will change on the falling edge of the clock and your register should shift on the rising edge.

\( y \) is the serial output (ie the 2’s complement bits)
\( \text{data} \) is a number to load the shift register with,
when \( \text{load} \) is high this data is stored on rising clock edge.

when \( \text{load} \) is low \( \text{shift\_control} \) high tells the register to shift and output the next bit in \( y \)

Your design should store 0 on the negative edge of the reset signal.