Question 2.1

@ After execution of the following instructions
@ what value will be in the condition code flags?

00 2000A0E3  MOV  r0, #0x20
04 2010A0E3  MOV  r1, #0x20
08 002051E0  SUBS r2, r1, r0

(A) 0xC   (B) 0x6   (C) 0x4
(D) 0x1   (E) 0x3   (F) OTHER

Question 2.2

@ After execution of the following instructions
@ what value will be in the condition code flags?

00 0301A0E3  MOV  r0, #0xC0000000
04 0F12A0E3  MOV  r1, #0xF0000000
08 003051E0  SUBS r3, r1, r0

(A) 0x9   (B) 0x4   (C) 0x1
(D) 0xE   (E) 0x0   (F) OTHER

Question 2.3

@ After execution of the following instructions
@ what value will be in the condition code flags?

00 0201A0E3  MOV  r0, #0x80000000
04 0111A0E3  MOV  r1, #0x40000000
08 007051E0  SUBS r7, r1, r0

(A) 0x9   (B) 0x4   (C) 0x1
(D) 0xE   (E) 0x0   (F) OTHER

Question 2.4

@ After execution of the following instructions
@ what value will be in the condition code flags?

00 0A02A0E3  MOV  r0, #0xA0000000
04 0F12A0E3  MOV  r1, #0xF0000000
08 003091E0  ADDS r3, r1, r0
0c 002043E0  SUB  r2, r3, r0

(A) 0x1   (B) 0x2   (C) 0x5
(D) 0x3   (E) 0xA   (F) OTHER
CSU33D01 Microprocessor Systems

Test 2

Condition Code Flags

Endianness

Architecture is little endian.

ASCII Table

Conditional Branch Instructions

Summary of LDR/STR Addressing Modes

<table>
<thead>
<tr>
<th>Addressing mode</th>
<th>Syntax</th>
<th>W, B</th>
<th>H, SH, SB</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Immediate Offset</td>
<td>[Rn, #/&lt;offset&gt;]</td>
<td>✓</td>
<td>✓</td>
<td>address + Rn +/- offset</td>
</tr>
<tr>
<td>Register Offset</td>
<td>[Rn, +/-&lt;Rm&gt;]</td>
<td>✓</td>
<td>✓</td>
<td>address + Rn +/- Rm</td>
</tr>
<tr>
<td>Scaled Register Offset</td>
<td>[Rn, +/-&lt;Rm&gt;, shift &lt;count&gt;]</td>
<td>✓</td>
<td>✓</td>
<td>address + Rn +/- (Rm &lt;shift&gt; &lt;count&gt;)</td>
</tr>
<tr>
<td>Immediate Pre-Indexed</td>
<td>[Rn, #/&lt;offset&gt;!]</td>
<td>✓</td>
<td>✓</td>
<td>Rn + Rn +/- offset</td>
</tr>
<tr>
<td>Register Pre-Indexed</td>
<td>[Rn, +/-&lt;Rm&gt;!]</td>
<td>✓</td>
<td>✓</td>
<td>Rn + Rn +/- Rm address + Rn</td>
</tr>
<tr>
<td>Scaled Register Pre-Indexed</td>
<td>[Rn, +/-&lt;Rm&gt;, shift &lt;count&gt;!]</td>
<td>✓</td>
<td>✓</td>
<td>Rn + Rn +/- (Rm &lt;shift&gt; &lt;count&gt;) address + Rn</td>
</tr>
<tr>
<td>Immediate Post-Indexed</td>
<td>[Rn], #/&lt;offset&gt;</td>
<td>✓</td>
<td>✓</td>
<td>address + Rn</td>
</tr>
<tr>
<td>Register Post-Indexed</td>
<td>[Rn], +/-&lt;Rm&gt;</td>
<td>✓</td>
<td>✓</td>
<td>address + Rn</td>
</tr>
<tr>
<td>Scaled Register Post-Indexed</td>
<td>[Rn], +/-&lt;Rm&gt;, shift &lt;count&gt;</td>
<td>✓</td>
<td>✓</td>
<td>Rn + Rn +/- (Rm &lt;shift&gt; &lt;count&gt;) address + Rn</td>
</tr>
</tbody>
</table>