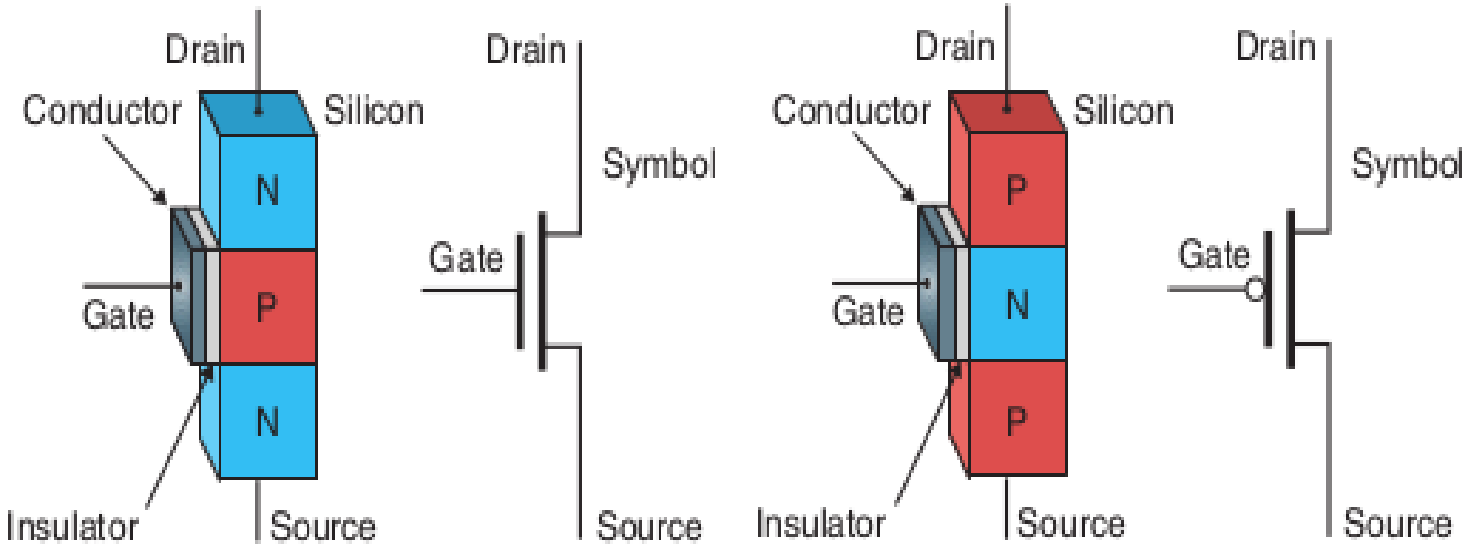
ENHANCEMENT-MODE MOSFETS



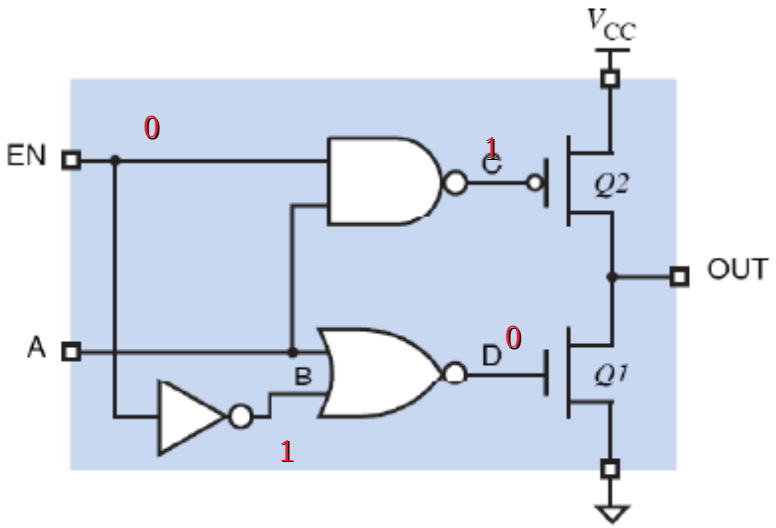
(a) NMOS field-effect transistor

(b) PMOS field-effect transistor

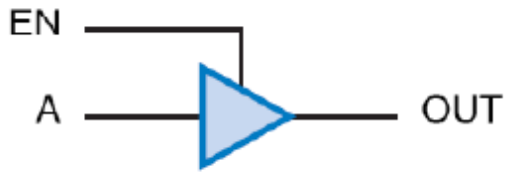
Source: **http://bit.ly/4nwwgJ5**

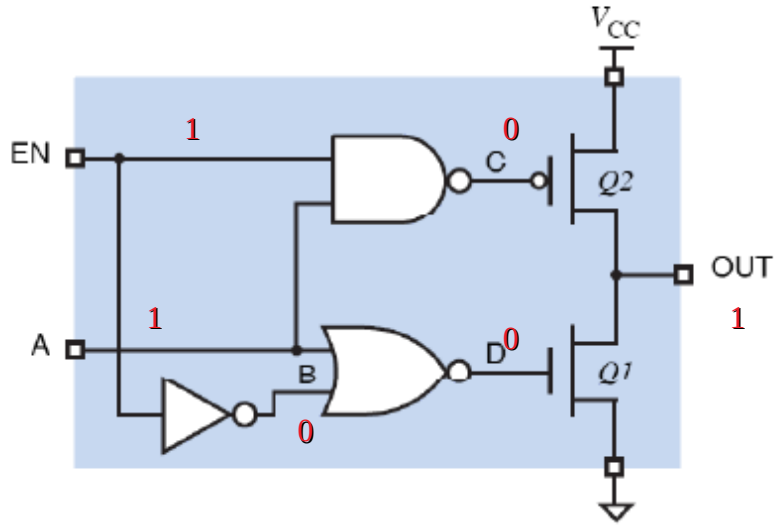
Three-state gates

Three-state gates may perform any conventional logic, such as AND or NAND. However, the one most commonly used is the buffer gate

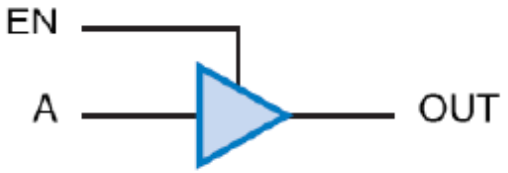


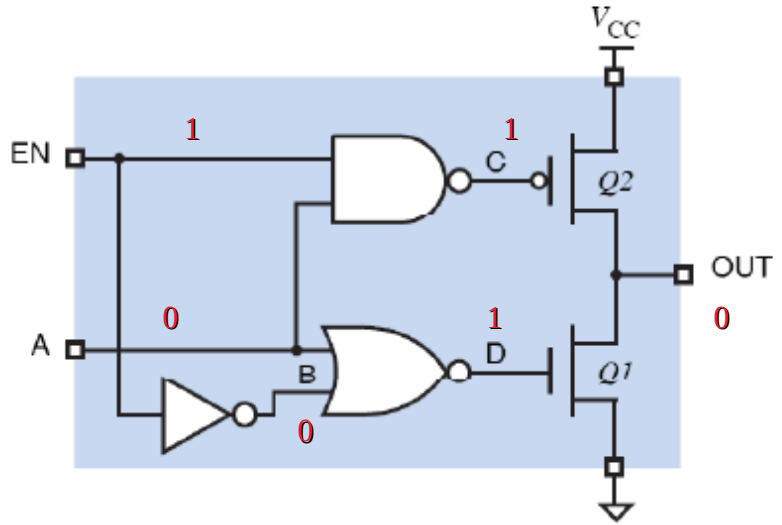
EN	A	B	C	D	*Q1*	*Q2*	OUT
L	L	H	H	L	off	off	Hi-Z
L	H	H	H	L	off	off	Hi-Z
H	L	L	H	H	on	off	L
H	H	L	L	L	off	on	H



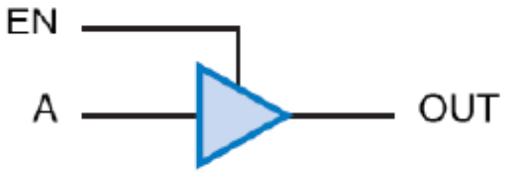


EN	A	B	C	D	*Q1*	*Q2*	OUT
L	L	H	H	L	off	off	Hi-Z
L	H	H	H	L	off	off	Hi-Z
H	L	L	H	H	on	off	L
H	H	L	L	L	off	on	H





EN	A	B	C	D	*Q1*	*Q2*	OUT
L	L	H	H	L	off	off	Hi-Z
L	H	H	H	L	off	off	Hi-Z
H	L	L	H	H	on	off	L
H	H	L	L	L	off	on	H



Three-state gates

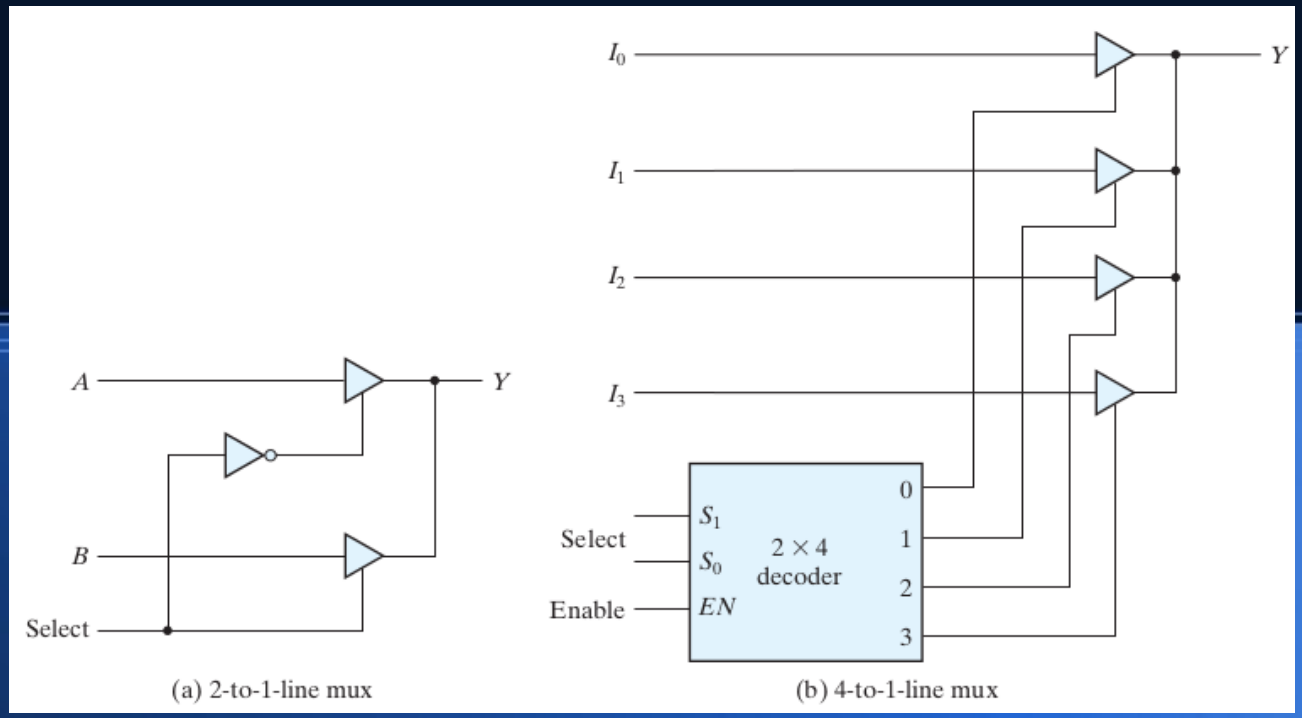
Two of the states are signals equivalent to logic 1 and logic 0 as in a conventional gate.

The third state is a high-impedance state in which
(1) the logic behaves like an open circuit, which means that the output appears to be disconnected,
(2) the circuit has no logic significance, and
(3) the circuit connected to the output of the three-state gate is not affected by the inputs to the gate.

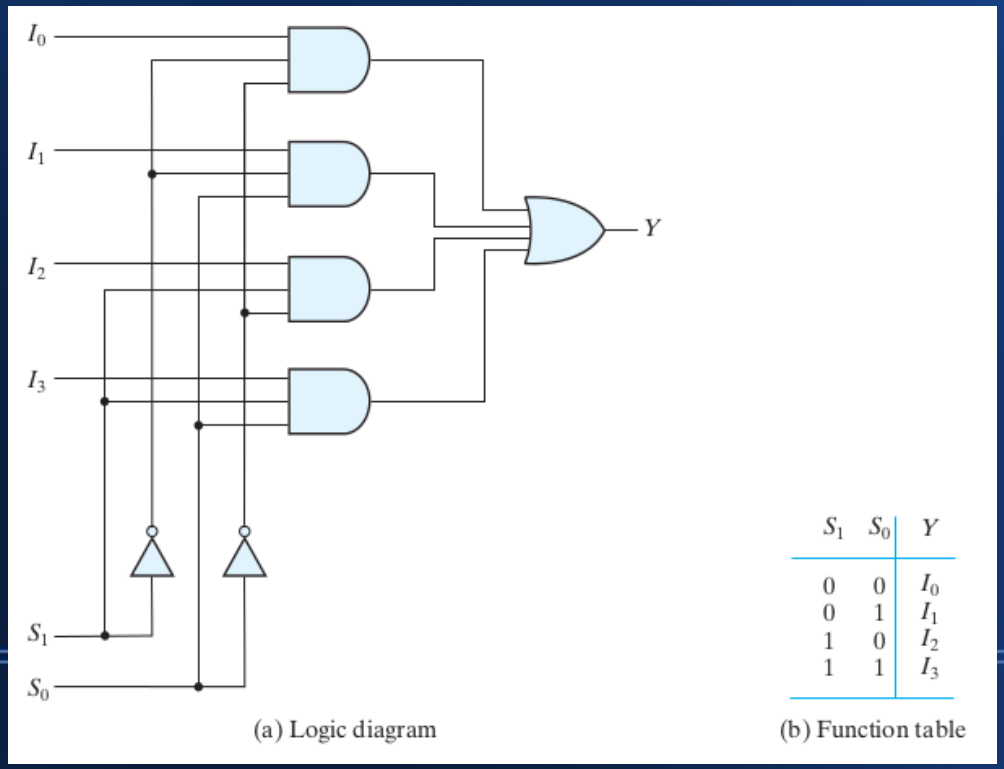
If more than one device is electrically connected, putting an output into the Hi-Z state is often used to prevent short circuits, or one device driving high (logical 1) against another device driving low (logical 0).

Three-state buffers can also be used to implement efficient multiplexers, especially those with large numbers of inputs. (Don’t need an OR gate with a huge number of inputs)

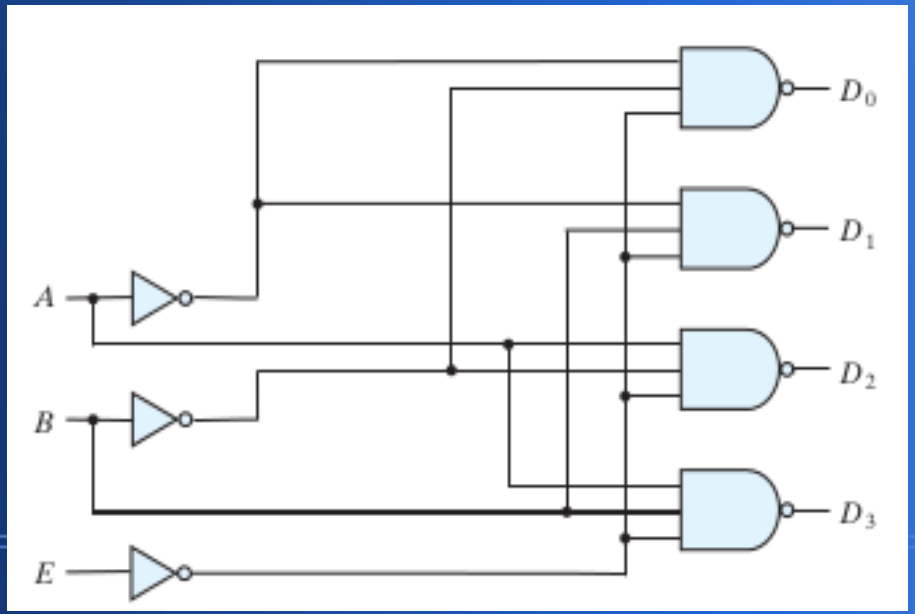
Multiplexers with three-state gates



4 x 1 mux



2 to 4 decoder



The construction of multiplexers with three-state buffers.

The construction of a two-to-one-line multiplexer with 2 three-state buffers and an inverter:-

The two outputs are connected together to form a single output line. (Note that this type of connection cannot be made with gates that do not have three-state outputs.)

When the select input is 0, the upper buffer is enabled by its control input and the lower buffer is disabled.

Output Y is then equal to input A. When the select input is 1, the lower buffer is enabled and Y is equal to B

The construction of a four-to-one-line multiplexer

The outputs of 4 three-state buffers are connected together to form a single output line.

The control inputs to the buffers determine which one of the four normal inputs I0 through I3 will be connected to the output line.

No more than one buffer may be in the active state at any given time.

The connected buffers must be controlled so that only 1 three state buffer has access to the output while all other buffers are maintained in a high impedance state using the decoder.